REMARKS

This Response concerns the Notice of Non-Compliance issued July 24, 2006, issued by the Examiner because claim 8 of the Amendment filed April 24, 2006 was not properly identified as "Currently amended". This response repeats the Amendment of April 24, 2006 with the correction to claim 8. Applicants have also amended the cover sheet of this Amendment to properly state that the Remarks begin on page 5 (rather than page 6, as incorrectly stated in the previous Amendment).

The Examiner has rejected claims 8-12 under 35 U.S.C. §112, second paragraph, as being indefinite. Applicants have corrected the antecedent basis as specified by the Examiner.

The Examiner has rejected claims 1-5, and 7 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 5,906,000 to Abe in view of U.S. Pat. No. 4,814,974 to Narayanan. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claims 8, 9 and 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claim 10 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland and further in view of David Eck (xLogic CircuitsLab 2: Memory Circuits). Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

The Examiner has rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Pat. No. 4,814,974 to Narayanan in view of U.S. Pat. No. 4,818,932 to Odenheimer and U.S. Pat. No. 5,581,722 to Welland and further in view of U.S. Pat. No. 5,918,160 to Lysejko. Applicant has reviewed these references in detail and does not believe that they disclose or make obvious the invention as claimed.

Applicant notes with appreciation that the Examiner has indicated that claim 6 would be allowable if rewritten in independent form.

With regard to claim 1, Abe does not show any element of the claim. As previously noted, the Abe reference is directed to a *cache controller* for use with a *single CPU*. Each entry in the cache memory 18 contains a tag area and a data area. The tag area (Figure 2) includes a valid/invalid flag 40 for the entry, a priority 42 for the data in the data area and an address indicative of the original location of the data (col. 4, lines 16-21). The priority for an entry is indicative of the frequency of access by the CPU 10 for accessing the data stored in the entry (col. 3, lines 61-64).

A cache memory stores a small subset of a main memory in a high speed memory to allow faster access to data from the main memory that has already been read. As more memory locations are read, some entries in the cache memory will be replaced with data from a different main memory location. The "priority" in the cache memory 18 of Abe is used to determine whether data from a currently read memory location in main memory *will replace the presently stored entry in the cache* (column 5, lines 38-51). No priority is used to arbitrate between multiple pending requests.

Abe does not show any method for prioritizing access to a shared resource in a digital system having a plurality of devices vying for access to the shared resource. As previously stated, Abe does not show a system with a plurality of devices, nor does it show shared resources.

Abe does not show a step of organizing an address space of the shared resource into address space regions. There are no shared resources in Abe – the main storage 20, ROM 32 and auxiliary storage 26 are only accessible by CPU 10. Further, Abe does not provide any organization of the address space of these various storage systems into regions.

Abe does not show the step of initiating an access request by a first device of the plurality of devices, wherein the access request specifies a target address within the address space of the shared resource. The only device in Abe that can issue an access request is the CPU 10.

Abe does not show the step of providing an access priority value with the access request, such that the access priority value corresponds to the access priority value assigned to the address space region selected by the target address. In Abe, there are no priority values within an access request. There would be no point in providing a priority value, since there is nothing to arbitrate. The priority value in Abe is used solely to determine whether a cache entry should be overwritten with information obtained pursuant to a cache miss.

Abe does not show the step of arbitrating between multiple pending requests to the shared resource for access to the shared resource based at least in part by using the access priority value assigned to each pending request. There are no "multiple pending requests" in Abe and, hence, no arbitration.

Narayanan does not cure any of the deficiencies of Abe. Narayanan teaches a *device-based* priority scheme where a priority for each device is assigned by a priority designator. When requesting access to a shared device, a REQUEST line (31-46) associated with the requesting system device is asserted. An arbitrator 27 selects one of the requesting devices through a GRANT line or lines (col. 4, lines 8-42). The arbitrator

27 selects among the requesting devices based on priority level uniquely associated with the devices.

As such, Narayanan does not show the step of organizing an address space of the shared resource into address space regions, nor does Narayanan show the step of assigning individual access priority values to a plurality of the address space regions. Narayanan does not have any address based priority levels, since each system device has a unique priority which is used to arbitrate between conflicts.

Narayanan does not show the step of providing an access priority value with the access request, such that the access priority value corresponds to the access priority value assigned to the address space region selected by the target address. In fact, Narayanan does not pass any priority value with an access request.

Narayanan does not show the step of arbitrating between multiple pending requests to the shared resource for access to the shared resource based at least in part by using the access priority value assigned to each pending request. As stated above, Narayanan does not pass priority values with the pending request, nor does it use a priority value assigned to the address space region selected by the target address.

Thus, even in combination, Abe and Narayanan do not show the key elements of claim 1. Neither reference assigns individual priority values to a plurality of address space regions and neither reference provides an access priority value with an access request to a shared resource. Neither arbitrates between pending requests based on the priority value associated with each pending request.

With regard to independent claim 8, Narayanan does not show a plurality of memory management units (MMU) each connected to receive an address from a respective one of the plurality of devices, wherein each MMU has storage circuitry *for storing a plurality of page entries and each page entry has an access priority value*, each

MMU being operable to output the *access priority value associated with a received address*. Specifically, as discussed above, Narayanan does not have any teaching of access priority values based on page entries, or any other address region.

Additionally, Narayanan does not show arbitration circuitry connected to receive a request signal from each of the plurality of devices *and the associated access priority value* from each MMU, wherein the arbitration circuitry is operable to schedule access to the shared resource according to the access priority values.

Neither Odenheimer or Welland cure the deficiencies of Narayanan. The Examiner states that an access priority associated with a received address is output by Odenheimer. It is clear from the cited passages of Odenheimer (col. 9, lines 4-8 and col. 15, lines 52-54) that the priority value used to arbitrate between competing memory access is *not* based on the address in the access request, but, instead, upon the *type* of access (a memory refresh message is given the highest priority and an access request for a message to the digitizer is given the next highest priority). Odenheimer has no teaching of the arbitration between memory accesses of the same type. Welland is used by the Examiner to show multiple MMUs and does not add any subject matter that would change the prioritization scheme of Narayanan or Odenheimer.

Accordingly Claim 8 is novel and unobvious over the cited references. Accordingly, Applicant asks for allowance of claim 8 and dependent claims 9-12.

The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is

respectfully requested that the Examiner telephone Alan W. Lintel, Applicant's Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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